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DATA RETRIEVAL AND PROCESSING SYSTEM

A USER'S GUIDE

by

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Hamilton Standard

Division of United Aircraft

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) This report defines the design of a specialized data retrieval system for logging analog data recorded on magnetic tape. It contains a description of the system, system interconnections, a list of equipment, and calibration and service procedures.		

FOREWORD

The original work that resulted in the Data Retrieval and Processing System was conducted by the Hamilton Standard Division of United Aircraft under Contract No. DA-19-129-AMC-603(N), Project No. 1K643324D587. Project Officer and Alternate Project Officer for the U. S. Army Natick Laboratories were Mr. Matthew Venetos and Mr. Denis O'Sullivan, both formerly of the Engineering Sciences Division of the General Equipment and Packaging Laboratory.

Subsequent investigations and refinements, funded under Project No. 1J662708D552, were conducted by Mr. Clive Nickerson, Principal Investigator, formerly of the Engineering Sciences Division of the General Equipment and Packaging Laboratory.

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DATA RETRIEVAL AND PROCESSING SYSTEM

A USER'S GUIDE

INTRODUCTION

This system is intended to reproduce data acquired by magnetic tape recorders installed in shipping containers. The parameters recorded are impact velocity, temperature, humidity, static force and dynamic load as a function of time.

Data is recorded in form of pulses whose amplitude and polarity is proportional to the parameter being measured.

Recordings are made with the tape in stationary position. The tape moves 1.6mm between data pulses.

Impact height is computed by the system from the three axis impact height components.

This data retrieval system accepts four parallel data channels which are recorded on magnetic tape. Three of these contain analog data and the fourth channel contains timing information. Each analog data point consists of either a positive leading and a negative lagging or a negative leading and a positive lagging pulse in which the peak magnitude is proportional to some physical quantity. The amplitude and polarity of the leading data pulse is recognized, measured and recorded by the system. A fourth analog data channel is generated in the system by combining the height vectors from the three height channels. At least one of the four input channels from the tape must contain information before the system will generate a read command. An uncertainty of pulse polarity and amplitude exists when first starting the system. Therefore, the first data point into the system from the tape after start-up is used to reset the system to its "ready" state and consequently is not recorded.

GENERAL DESCRIPTION

The system consists of a control panel, a tape playback unit, a programmer, an analog-to-digital converter, a high-speed electro-optical printer and power supply racks.

With the exception of the programmer and the control panel, all equipment was commercially available.

The programmer serves to interface and control the various equipment. Some special circuitry used in this unit for signal conditioning and control are built on plug-in boards similar to the purchased logic plug-in boards.

SPECIFICATIONS

1. Input voltage range to programmer ± 0.137 to $\pm 2V$.
2. Tape playback speed 1-7/8 IPS (4.75cm/sec).
3. Logging Rate - 30 Lines/Sec./150 data channels/Sec. nominal - 100 Lines/Sec. maximum.
4. System accuracy $\pm 1\%$ FS (excluding tape playback equipment).
5. Linearity $\pm 1\%$ FS best straight line.
6. Stability $.05\%$ /Day constant temp.
 $.01\%/^{\circ}C$
7. Input power 105-135V, 10A at 60 HZ.
8. Number of input channels: 3 data channels plus time channel. A fourth data channel is generated internally by combining drop height vectors from the 3 input data channels.

In order that tape drop-out errors be reduced to a minimum, a high quality instrumentation tape should be used for recording the data.

THEORY OF OPERATION

For the discussion that follows refer to the system logical schematic 11-1-2505 and the timing diagram 11-1-2506 available in appendix.

A. POLARITY SENSE AND GATE GENERATION

Let it be assumed that the system is in the reset state, that a data point from channel 1 is entering into PB1A1 and that its leading pulse is positive. The pulse is amplified by the peak memory driver PB1A1 and applied simultaneously to the peak memories and the polarity sense zero crossing detectors. Operational trigger PB3A2 is biased to saturation by a negative bias potential, PB3A1 is biased to saturation by a positive bias. The positive incoming pulse will overcome the negative bias on PB3A2 and PB3A2 will switch states causing one shot PB24SS2 to generate a 5 microsecond pulse. This pulse is used for setting the positive peak memory store flip-flop, reset the system if this is the first data pulse entering the system after start-up, or initiate a print command through PB3OSS2.

The positive pulse that triggered PB24SS2 is also applied to PB3A1, but since this operational trigger is already saturated by a positive forward bias it will have no effect on the output of this operational trigger.

The 5 microsecond pulse from PB24SS2 is applied simultaneously to PB27NAND2 and PB32ACOR1-4. Input 9 of PB27NAND2 is forward biased by PB23FF1. The incoming pulse to pin 8 of PB27NAND2 will pass through PB27NAND2; PB23FF2 will be set and the positive peak memory will be unclamped which allows the storage capacitors in the memory to charge the peak amplitude of the positive incoming pulse. A short time later the negative pulse of the data will trigger PB3A1 by overcoming its positive bias, PB3A1 will switch states and generate a 5 microsecond pulse via PB24SS1. This pulse, however, is ignored since PB27NAND1 is inhibited by PB23FF2 being in the set state. For a negative initial pulse PB23FF1 would be set first and would inhibit PB27NAND-2 and the positive peak memory.

B. INITIAL SYSTEM RESET

The system becomes operational when SW3 is actuated. SW3B opens to forward bias PB20NAND5 to permit control gates to initiate printing action, and SW3A closes to discharge C1. When C1 discharges, a pulse is generated that resets PB26FF3 and triggers PB51SS3 to generate a 15 microsecond reset pulse that is applied to all flip-flops and the printer. This pulse closes the peak memory clear gates and resets them to zero. It resets the sequencing flip-flops in the multiplexer so that switch Ch1 is closed and it resets the printer to column number 1. The first pulse from PB32ACOR1-4 will set PB26FF3 and trigger PB3OSS2. In setting, PB26FF3 will trigger PB3OSS1. A 10 millisecond pulse

is applied to pin 6 of PB20NAND5 from PB30SS1, via PB31IA1. The 10 millisecond pulse inhibits PB20NAND5; hence the first initial print command is inhibited. The lagging edge of the 10 millisecond pulse triggers PB51SS3 to generate a reset pulse for resetting the peak memories that may have been charged up by the first data pulse.

C. PRINT CYCLE

Subsequent pulses coming from PB32ACOR1-4 will not affect PB26FF3, but these pulses will trigger 2 millisecond time delay PB30SS2. The function of this time delay is twofold. First, it gives sufficient delay for the counter to register the timing pulse and second, it gives the peak memory sufficient time to charge to the peak value in the event of tape head misalignment.

At the end of the two-millisecond delay PB30SS3 is triggered and generates a 5 microsecond pulse which resets and sets PB26FF4. In setting, PB26FF4 triggers PB51SS2 via PB45DCOR5, PB31IA3 and PB51SS1. The output of PB51SS2 is the print command to the printer. Upon receipt of the initial print command, the printer prints column No. 1 which is the thousands digit for the time. It is obvious that more than one pulse can come from PB32ACOR1-4 in any given print cycle. But only the first pulse initiates the print cycle because once PB26FF4 sets, additional pulses to its set input have no effect on its state.

When the printer is reset, it moves to column No. 1, PB33AND1 is activated, and it in turn activates gates PB46AND5 through PB46AND8 to couple the binary bits of the thousand digits on the time counter to the printer via DCOR gates PB42DCOR2 through PB45DCOR2. After printing the thousand digits in column No. 1, the printer will move to column No. 2; in doing so PB33AND1 will be inhibited and PB33AND2 will be activated. Gates PB46AND5 through 8 will be inhibited and gates PB46AND1 through 4 will be activated and binary information of the 100 units of the time counter is coupled to the printer. On activation, PB33AND2 will also trigger 10 microsecond delay PB51SS1; after 10 microseconds PB51SS2 is triggered which in turn generates a print command, so that binary information on column No. 2 is printed. The 10 microsecond delay of the print command is necessary to allow binary information coupled to the printer to reach steady state. Upon printing of column No. 2, columns No. 3 and 4 (10's and units) will be printed in similar manner. After column No. 4 has been printed, PB33AND4 is inhibited, and PB34AND1 is activated. A digitize command is now applied to the ADC converter through PB45DCOR. Upon receipt of this command, the ADC will digitize the data of channel No. 1. After completion of the digitization cycle, the ADC delivers a "space" command to the printer. The printer leaves a blank on column 5 and moves to column 6. Gate PB34AND2 will now be activated which in turn will activate gates PB45AND1 through 4 to couple to the printer binary information representing polarity sign of the first channel. The 10 microsecond print command delay is also

triggered so that at the end of 10 microseconds the printer will print either a blank indicating a positive quantity or a minus sign for a negative quantity on channel No. 1. At the same instant the sign polarity gates PB40AND1 are activated, PB19FF1 is pulsed causing the sequencing flip-flops to open channel 1, the system will proceed to print the 100's, 10's and units on the ADC in a similar manner as for the time counter. On columns No. 10, 15 and 20, the ADC will receive a command to digitize and on columns 11 and 16 the sequencer will receive a command to step to channels 3 and 4 respectively.

If height data is not required, SW2 is set to the four channel mode. When the printer reaches column No. 20, the output of PB38AND4 is coupled to the reset line through PB42DCOR5, PB31IA2, and PB57DR2. The system now is reset; that is, the peak memories are discharged (set to zero); the multiplexer is set to channel 1; PB26FF4 sets to await the next initial print command, and the printer resets to a new line and column No. 1.

When height computation data is required, the system will print 5 channels of information, and system reset will occur when the printer reaches column 24.

The column decoder gates, PB33AND1 through PB39AND4, provide a digital feedback loop with positive control on the entire system. The entire system is reset for each line of recorded data and cannot remain out of synchronization for more than one line of printout.

DESCRIPTION OF EQUIPMENT

The Monroe MC400N optical printer is capable of printing up to 100 lines per second. It accepts four parallel bit characters serially with -12 volt true logic and 0V false logic. Printing is done on Kodak Linagraph Direct Print oscillograph paper, type 1855, Spec. 111.

The analog-to-digital convertor (ADC) is a Beckman Model 4040A which accepts 10 volts full scale input with a 1.33K per volt input impedance and has an 8-4-2-1 binary coded three-digit decimal output (13 binary digits including the sign). The output of this unit is also -12 volt true and 0 volt false. The maximum time per conversion is 51 microseconds.

Temperature and humidity plotter outputs are provided for graphically recording the history of a package over the time of shipment or storage. A Honeywell Electro Instruments Model 400 plotter is used with vertical differential amplifier (maximum sensitivity: 1 mv/inch) and time base (0.02 to 2 inches/sec.) plug-ins. Response of this unit is 3 db down at 5 Hz. Plots are made on 11 x 17 inch graph paper.

A description of the programmer and its function for system control and interfacing of equipment is given in the "Theory of Operation" section. For more detailed information on the other units, the manufacturers' manuals should be consulted.

DESCRIPTION OF PLUG-IN MODULES

A description and function of the analog modules and multiplex switch is given in this manual. Plug-in digital modules are described in the manufacturer's module manual which should be referenced whenever information is required on the digital modules. These modules are generally of the DTL type, using discrete components and -12 volt true and 0 volt false logic levels.

CONTROL PANEL - 11-1-2518

As the name implies, this unit provides the necessary controls for turning the power on and off, selecting the mode of operation, starting and stopping the system, and selecting the desired channel for monitoring on the scope.

On depressing the log/standby switch for the logging operation, the unit first starts the tape transport. After full speed is reached by the tape transport the unit resets the system and activates NAND gate PB20NAND5 in the programmer to allow logging operation. On setting the system on "standby", the print control gates are first deactivated, then the tape transport is turned off. This procedure avoids erroneous print-outs of data.

Control of the system is accomplished as follows:

When SW1 is pressed to the "log" position, C1 charges through SW1A CR1 and R2 and K1 energizes. SW1C closes and the contacts of K1 open to turn on the tape transport. C2 also charges, but at much lower rate, through R1 and CR2. After about one second delay, the voltage across C2 overcomes the zener voltage of CR3, and K2 is energized. K2 energizes mercury relay K3. When K3 is energized, pin No. 5 swings to -12V to activate the print control gate PB2ONAND5 in the programmer. Pin No. 3 is shorted to ground. C3 delivers a positive pulse to the programmer for resetting the system.

When SW1 is set to the standby position, K3 de-energizes. PB2ONAND5 in the programmer is inhibited, thus preventing initial print commands from reaching the printer. The charge on C1 prevents K1 from de-energizing until a few milliseconds later. This guarantees that the tape transport is always at full speed while the system performs the logging operation. Mode control is accomplished through SW2A and SW2B by connecting the reset gate to the proper column on the column decoder gate. Deck SW2C switches the correct scaling factor the output amplifier, thus minimizing calibration time when switching tapes.

The lines of SW4 terminate to the output of the tape preamplifier. The arms of SW4 terminate to the oscilloscope, thus permitting channel monitoring.

SW3 is the time override switch. If it is necessary to stop the logger and restart it on the same tape, SW3 is set to "off" position. This will prevent the time counter from resetting to zero when restarting the logger.

PEAK MEMORY DRIVER - 11-1-2508

This unit amplifies the incoming signal and has enough drive capability to rapidly charge the peak memories without overloading. It also drives the zero crossing detectors.

It consists of an operational differential amplifier A1 whose gain is fixed by R1 and R2. The gain of this amplifier is equal to $(R1 + R2)/R1$. A 1.5-volt signal to the input will give a full scale reading on any scale. The three boards this unit drives must be D.C. isolated from each other. Capacitors C1 to C3 are used to provide this isolation.

PEAK MEMORIES - 11-1-2515

This circuit is used for storing the data pulse amplitude until logging is completed.

The peak memories consist of rectifier diodes for polarity sensing, integrated chopper for clamping and an operational voltage follower. The rectifiers CR5 and CR6 are forward biased with approximately 0.4VDC to

overcome the diodes forward barrier voltage. This bias is obtained from the $15 \pm$ volt supplies and is developed across CR2 and CR4. The change in the voltage drop across CR2 and CR4 with temperature, temperature compensates the rectifiers.

Assuming a positive leading data pulse, the bases of Q1 and Q3 will be driven positive. This will cut off Q1 and Q3 and allow the peak memory capacitors C1 and C2 to charge to the peak value of the incoming pulse. One half of the amplitude is applied to the operational voltage follower. The output of this unit is the data signal applied to the ADC via the output amplifier.

For a negative leading data pulse, the negative switches Q2 and Q4 open to allow C3 and C4 to charge.

At the end of the logging cycle the bases of Q1 and Q3 are driven positive. Q1 and Q3 conduct to discharge the peak memory capacitors C1 and C2. The function of Q3 and Q4 is to prevent the operational followers A1 and A2 from drifting due to leakage currents that can flow into C1 and C3 from A1 and A2 respectively.

Resistors R6, R7, R11 and R15 serve to limit the discharge currents from the peak memory capacitors into the integrated choppers. R5 and R14 limit the charging current that can flow from the peak memory driver.

The peak memories are capacitively coupled to the peak memory driver. The coupling capacitors accumulate a small charge during the leading data pulse. R1 CR1 and R9 CR3 act to remove this charge during the lagging data pulse period.

The peak memory is adjusted for zero output with zero input as follows:

Apply power and let stand 1/2 hour. Remove the tape that may be on the tape deck and depress the "Log" switch. Adjust R8 and R16 for zero output at TP1 and TP2.

ZERO CROSSING DETECTORS - 11-1-2510

These units sense the polarity of the incoming pulse and perform a switching function when the incoming pulse exceeds 0.137 volts. The output pulse from these units is used for opening the peak memories and to initiate a readout cycle.

Each unit consists of two high-speed, high-gain differential amplifiers in a positive feedback loop. The output of these amplifiers switches rapidly from plus to minus or from minus to plus when the input exceeds a certain threshold.

The threshold voltages of 0.137 volts are obtained from the ± 15 V supplies and voltage dividers R1, R2, R3 and R4.

A1 is biased with 0.137 V from the junction of R1 and R2. Positive feedback is applied to this unit from the junction of R10 and R11. With zero input to pin No. 8, the output of A1 is at the -11 to -14 volt level. When a negative input voltage to pin No. 8 exceeds the positive threshold voltage of 0.137 by about 10 MV, the output of A1 switches from minus to plus 11 to 14 volts.

A2 is biased with a negative bias of 0.137 V. Its output with zero input is +11 to +14 V. When the input to pin 8 is greater than 0.137 volts, A2 switches from plus to minus 11 to 14 V. An inverter consisting of Q1, CR5, R16, R17 and R15 follows A2. It is necessary to invert the pulse from A2 since the logical circuitry following these units responds to positive going pulses.

CR1 through CR4 prevent damage to the amplifier through excessive input voltages.

This unit is initially adjusted as follows:

With power applied, the plus and minus inputs of each amplifier are shorted to the common. R9 and R8 are then adjusted until the output of each amplifier is zero, as measured at TP1 and TP2.

OUTPUT AMPLIFIER - 11-1-2512

This unit combines the negative or positive data input from the peak memories and provides the necessary scaling of voltages for readout in engineering units by the ADC.

The input data voltage is divided by R1, R2 and R4 and is reamplified by A1 to the proper level. The correct scale factor is selected by energizing one of the three relays. This connects the feedback resistors around the amplifier for proper scaling.

The gain of the amplifier at either input while the other is shorted is given by

$$A = \left(\frac{R5 + Rf}{R5} \right) \left(\frac{R4}{R_{in} + R4} \right)$$

Where Rf is the feedback resistance, R6 + R7, for example. When K2 is energized, the amplifier is scaled to read temperature in degrees F.

With zero input the amplifier output is -.5 V representing -50°F. The transfer function of the amplifier under the "temperature" mode is given by

$$E_o = .25 (E_i - 2.0)$$

The 2.0 V offset is provided by the R12 - R13 divider. Negative tem-

peratures from -50°F through -1°F will print out 950 through 999. Subtract print-out from 1,000 to determine the correct value in this range.

These units are initially adjusted as follows: Pins 8 and 10 are shorted to common. R3 is then adjusted for zero output on pin 16.

An adjustable zero offset is provided in the drop height playback mode to compensate for any apparent negative offset caused by the non-linearity on the lower part of the drop height-playback voltage.

Adjustment procedure is as follows:

1. Graphical determination of intercept of drop height-playback voltage curve by extension of linear portion of the curve through the zero drop height line.
2. Computation of equivalent print-out from the intercept value. Print-out = $320 \times \text{Intercept (volts)}$.
3. Setting of the extra potentiometer (mounted on an operational amplifier) on PB9 so that with zero input into PB4, PB9 and PB14, the print-out in channels 1, 2 and 3 agrees with the determined print-out.

For calibration of these units refer to the calibration procedure.

MULTIPLEX SWITCH - 11-1-2517

This unit sequentially connects the four data channels to the ADC for digitalization.

The inputs from the sequence NAND gates are fed to the integrated chopper bases. The logical connection to the sequence NAND gates are such that only one integrated chopper is forward biased at any one time. When the system is in reset state, Q1 is forward biased with the remaining integrated choppers off.

The conducting chopper has an "on" resistance of about 10 ohms with a typical offset voltage between E1 and E2 of less than 5 MV. The "off" resistance of these units is greater than 500 megohms.

PEAK MEMORY SWITCH DRIVER - 11-1-2514

This circuit converts the memory set flip-flop voltage levels to those required for driving the integrated chopper clamp.

When Q1 and Q2 are off, their collector voltage swings to the +24 V supply, opening the integrated choppers in the peak memory.

The drivers are cut off when the input to the bases is between -9 to -12. They become saturated when the input to their bases is

at ground potential. When the drivers are driven to saturation, their collectors swing toward -9 V DC. This forward biases the integrated choppers in the peak memories and prevents the memory capacitors from charging.

Three similar units are built on a single plug-in board.

ARBITRARY FUNCTION CIRCUIT - 11-1-2511

This circuit has an adjustable transfer characteristic consisting of eleven straight-line segments whose slopes are set by potentiometric screwdriver adjustments on a Philbrick/Nexus SPFX-P arbitrary function transconductor module. The initial slope is fixed at 45° by a 20K resistor across pins 9 and 10 of the SPFX-P module. A differential subtractor amplifier (PBX01) is used to allow arbitrary conditioning of both positive and negative outputs of memory, and an additional inverting amplifier (PBX02) follows the module to allow both positive and negative changes in slope.

These features are incorporated into the read-out unit to allow compensation for non-linear playback behavior. Setting of the arbitrary function so that it is the inverse of the input function serves to linearize the overall characteristic.

The initial slope interval is between 0.0 and +0.5 volts input. Subsequent segments are in 1-volt input increments up to 9.5 volts. The final segment is from +9.5 volt to +10 volt input. The largest incremental slope change allowed is 0.4V/V.

The procedure for use of this circuit follows:

1. Draw the inverse of the function to be fitted.
2. Determine the incremental slope changes necessary to obtain the inverse.
3. Using the test card in place of the peak memory board in the channel to be adjusted, feed in a low frequency sine wave of 8 volts peak amplitude into the memory No. 1 terminal while grounding memory No. 2 terminal on test card.
4. Monitor input (sine wave) and output of arbitrary function circuit at test point on PB5, PB10 or PB15 using an X-Y oscilloscope display.
5. Adjust SPFX-P module by setting potentiometers 1 through 8 in order, so that the incremental slopes on the X-Y display agree with those determined for the function inverse.

SUMMING AMPLIFIER - 11-1-2509

This unit sums and scales height inputs. It performs the mathematical operation of

$$V_o = A (V_{11} + V_{22} + V_{33})$$

Where V_{11} , V_{22} and V_{33} are the voltages from the arbitrary function circuits, the output of this amplifier is then analog to

$$h = \frac{V_1^2 + V_2^2 + V_3^2}{2g} = h_x + h_y + h_z$$

The gain of this stage is given by

$$A = \frac{R_6 + R_7 + R_4}{R_4}$$

This unit is initially adjusted as follows: Pins 8, 9 and 10 are shorted to the common, and R_5 is adjusted for zero output at TPL. When shorting pins 8, 9 and 10 to common, be sure the arbitrary function circuits are removed or disconnected from these pins.

COLUMN GATE DRIVER - 11-1-2507

This circuit is used to increase the driving capability of the printer column decoder lines.

The driver is a Darlington, complementary push-pull emitter follower capable of driving 90 AND gates. CR1 and CR2 provide a slight forward bias to the drivers, Q2 and Q3, to increase the unit's speed of response. In the event the drop across the biasing diodes is high compared to the forward base drop of Q1 and Q2, R4 limits the collector current of Q1 and Q2 from becoming high while the driver is in its quiescent state. R1 limits the power dissipation and collector current of Q2. The voltage gain of this circuit is between 0.85 and 0.95 with 0 to -10 V at the base of Q1 and a 120 ohm load at the output.

CALIBRATION PROCEDURE

After a half-hour warmup period the read-out unit should be calibrated according to the following procedure:

1. Zero amplifiers in the following sequence with the inputs to channels 1, 2 and 3 all shorted to ground.

- a. Input amplifiers (PB1, PB6, PB11)
- b. Memories (PB2, PB7, PB12)
- c. PBX01 outputs (use test card)
- d. PBX02 outputs (use test card)
- e. Arbitrary function output (PB5, PB10, PB15)
- f. Output amplifiers (PB4, PB9, PB14) (Set to load mode and use test card.)
- g. Summing amplifier (PB16) (Set to load mode.)

2. Check and adjust the arbitrary functions using a sine wave input into the test card for linear transfer characteristics or adjust to the desired non-linear characteristics.

3. Check and adjust the offset for zero in the drop height mode or adjust to desired offset.

4. Set the mode switch to drop height and feed in a 1.5 volt, 400 microsecond, 30pps pulse train into channel number 1 while other channels are shorted.

5. Adjust the output amplifier (PB4) drop height potentiometer and the summing amplifier (PB16) potentiometer for print-outs of 480.

6. Repeat 1. through 5. for channel 2 (PB9) and channel 3 (PB14).

7. Switch to the temperature/humidity mode.

8. Feed the above signal into channel 1 and adjust the output amplifier (PB4) temperature potentiometer for print-out of 150.

9. Feed into channel 2 and adjust for a print-out of 100.

10. Feed into channel 3 and adjust for a print-out of 600.

Before each use of the read-out unit to retrieve drop height or temperature/humidity static load information, the playback tape deck output amplifiers should be adjusted to yield 1.5 volts out for the following recorded information that is applicable:

Drop Height	48 inches (122cm)
Temperature	150°F (65.6°C)
Humidity	100%
Static Load	6,000 pounds (2,718 Kg)

OPERATING INSTRUCTIONS

1. Turn on power on all equipment and allow 1/2-hour warmup on standby mode.
2. Place data tape on tape deck.
3. Place all tape deck push button controls on their "off" position.
4. Select the mode of operation to correspond to the data tape with the mode selector switch on the control panel.
5. Depress the standby-log switch to the log position for commencing the logging operation.
6. The system will automatically cease logging when the tape reel is finished.
7. To stop the logging cycle, depress the standby-log switch to the standby position.

TROUBLE SHOOTING

Trouble shooting time can be shortened considerably if it is well understood how the system functions. Therefore, the system description and logical schematic should be carefully studied. Once the system is well understood, "effect-to-cause" reasoning and through waveform observation at various test points provided should quickly locate the defect.

The first steps in trouble shooting should be to check all power supply outputs. In many cases, a readjustment of power supply settings will correct the malfunction.

Because semiconductors are used exclusively, resistance measurements on a normal or defective circuit can exhibit a wide range of deviations, depending on the ohmmeter used, polarity connections, and the ambient temperature. Resistance measurements are not recommended. A good oscilloscope with 2 or more simultaneous traces is the most effective service tool for localizing the trouble.

The defective circuit or unit can be easily traced by referring to the timing waveform diagram drawing 11-1-2506 and 11-1-2516.

When trouble is located in one of the commercial units, the manufacturer's manual for that particular unit should be consulted.

It is recommended that the circuit used for calibrating the system be also used for trouble shooting. The normal waveforms at various test points specified on 11-1-2516 with the input data pulse on channel 1 are shown on this drawing.

If printing action stops after printing the time channel or at columns No. 5, 10, 15 and 20, the trouble is either with the column decoder or the ADC. If no readout occurs or the system stops at some other column, the trouble is either in the column decoder or the printer.

With a negative input data pulse, waveforms No. 1 and 2 on 11-1-2516 are reversed in polarity.

Waveform No. 2 appears on PB2TP2. Waveforms 3 through 6 appear on PB3TP1, PB24TP3, PB27TP6 and PB23TP4, respectively.

Waveforms 7 through 21 will appear at the same test points, regardless of the channel being tested or the polarity of the input data pulse.

The waveforms shown on timing diagram 11-1-2506 are essentially the waveforms that appear on the column decoder. Waveform No. 1, for example, should appear on PB33TP6. Waveform No. 5 appears on PB34TP1, PB37TP6, PB38TP4 and PB39TP4 with one pulse on each test point for every readout cycle.

The table which follows lists the programmer test points for waveforms 1 to 6 for checking out the three channels with negative and positive data pulses. All waveforms should have similar characteristics shown on 11-1-2516, except waveforms 1 and 2 should be reversed in polarity with negative input data pulses.

Input Data Pulse	Waveform No.					
	1	2	3	4	5	6
Ch. #1 Pos.	PB1TP1	PB2TP1	P33TP2	PB24TP2	PB27TP5	PB23TP3
Ch. #1 Neg.	PB1TP1	PB2TP2	PB3TP1	PB24TP3	PB27TP6	PB23TP4
Ch. #2 Pos.	PB6TP1	PB7TP1	PB8TP2	PB24TP1	PB27TP3	PB23TP1
Ch. #2 Neg.	PB6TP1	PB7TP2	PB8TP1	PB25TP3	PB27TP4	PB23TP2
Ch. #3 Pos.	PB11TP1	PB12TP1	PB13TP2	PB25TP1	PB27TP1	PB26TP3
Ch. #3 Neg.	PB11TP1	PB12TP2	PB13TP1	PB25TP2	PB27TP2	PB26TP4

DATA RECORDING AND PLAYBACK

It is recommended that the recording head gap be 0.001" (.025mm). A wider gap will cause cross talk between channels and partial erasure from data point to data point.

A smaller recording head gap will reduce the pulse width. This will require shorter peak memory responses, which could result in poorer noise rejection by the system and also increase tape dropout errors.

The reproduce heads should have a narrow gap for good high frequency response. The 4-channel standard playback heads as installed by Precision Instruments on their tape transport units are satisfactory in this respect.

LIST OF PLUG-IN MODULES REQUIRED FOR PROGRAMMER

Programmer cabinet is Raytheon MCR-75-500

<u>Type</u>	<u>No. Required</u>		<u>Drawing or Manufacturer</u>
GDG2-.2	10	Diode AND Gate	Raytheon
GDG3-.2	4	D.C. OR Gate	Raytheon
GFF1-.2	3	Flip-Flop	Raytheon
GLG1-.2*	2	A.C. OR Gate	Raytheon
GOS3-.2	4	One Shot	Raytheon
GNA1-.2	2	NAND Gate	Raytheon
GST2-.2	1	Schmitt Trigger	Raytheon
GDC1-.2	4	Decade Counter	Raytheon
GAI2-.2	1	Inverting Amplifier	Raytheon
GRG1-.2	1	Reset Gate	Raytheon
700125	3	Peak Memory Driver	Hamilton Standard
700131	1	Peak Memory Switch Driver	Hamilton Standard
700132	3	Peak Memory	Hamilton Standard
700127	3	Zero Crossing Detector	Hamilton Standard
700128	3	Arbitrary Circuit	Hamilton Standard
700126	3	Summing Amplifier	Hamilton Standard
700129	1	Output Amplifier	Hamilton Standard
700134	2	Multiplex Switch	Hamilton Standard
700124	4	Column Gate Driver	Hamilton Standard
700137	1	A.C. OR Gate	Hamilton Standard
700139	1	Low Pass Filter	Hamilton Standard

*One of these gates is modified per Drawing 11-1-2520.

LIST OF DRAWINGS AND MANUALS

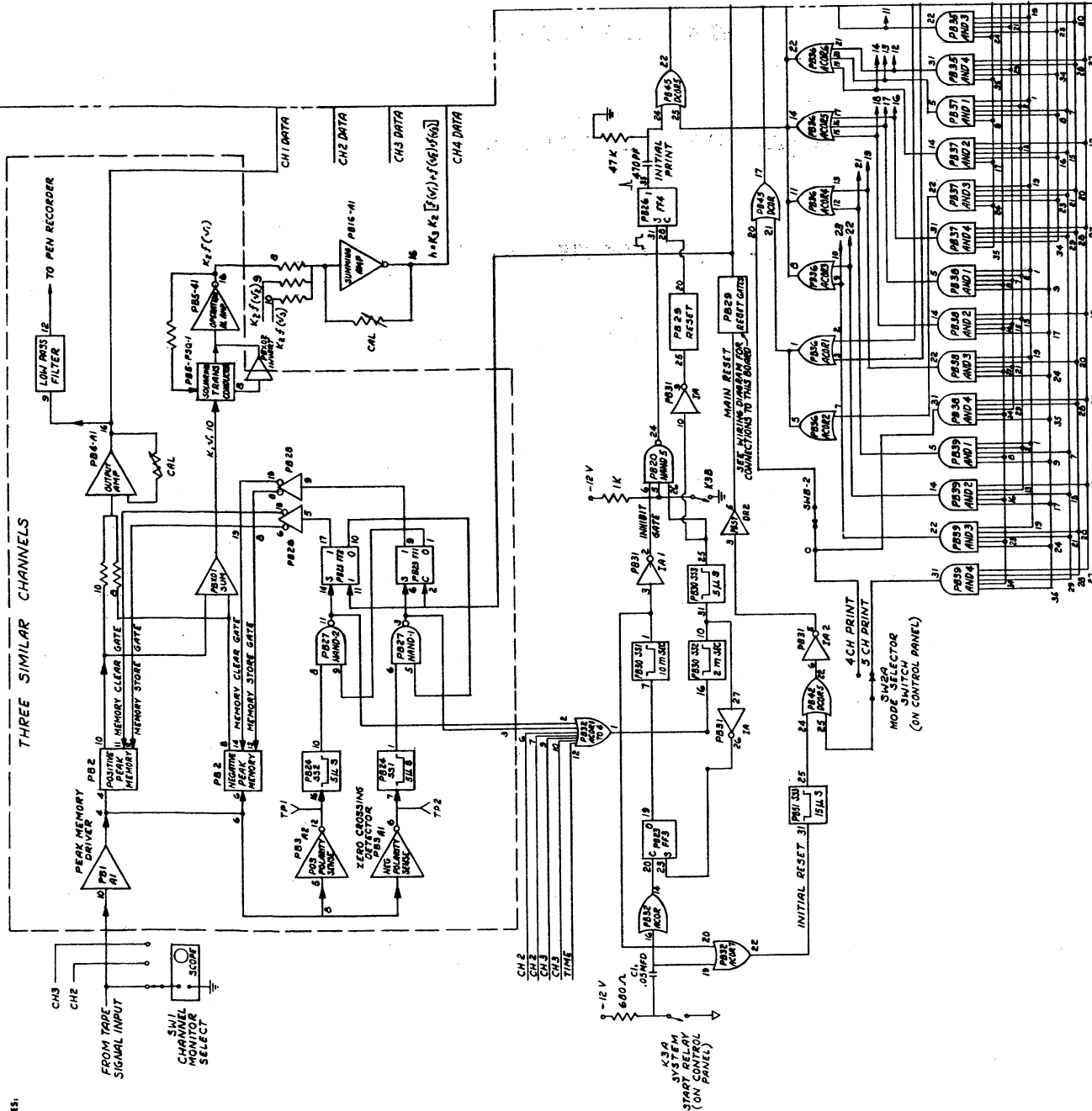
<u>Number</u>	<u>Title</u>
11-1-2505	System Logical Schematic
11-1-2506	Timing Diagram
11-1-2507	Column Gate Driver PB48, PB49, PB50 and PB57
11-1-2508	Peak Memory Driver PB1, PB6 and PB11
11-1-2509	Summing Amplifier PB16
11-1-2510	Zero Crossing Detector & Gate Generator PB3, PB8 & PB13
11-1-2511	Arbitrary Function PB5, PB10 and PB15
11-1-2512	Output Amplifier PB4, PB9 and PB14
11-1-2513	Programmer Power Supply Connections
11-1-2514	Peak Memory Switch Driver PB28
11-1-2515	Peak Memory PB2, PB7 and PB12
11-1-2516	Trouble Shooting Timing Diagram
11-1-2517	Multiplex Switch PB17 and PB18
11-1-2518	Control Panel
11-1-2519	Programmer Wiring Diagram
11-1-2520	A.C. OR Negative Input PB32
11-1-2521	System Wiring Diagram
11-1-2522	Recorder Filter PB21
Model 404DA	ADC Manual, Beckman Instruments
Model 4000	Printer Manual, Monroe Data/Log.
Model PI6001	Tape Transport Manual, Precision Instruments
Model SPFX-P	Arbitrary Function Transconductor Philbrick/Nexus
LM	Power Supply-Series-Specifications, Lambda Electronics
CPM 3001	Modules Manual - Raytheon

APPENDIX

ELECTRICAL SCHEMATICS

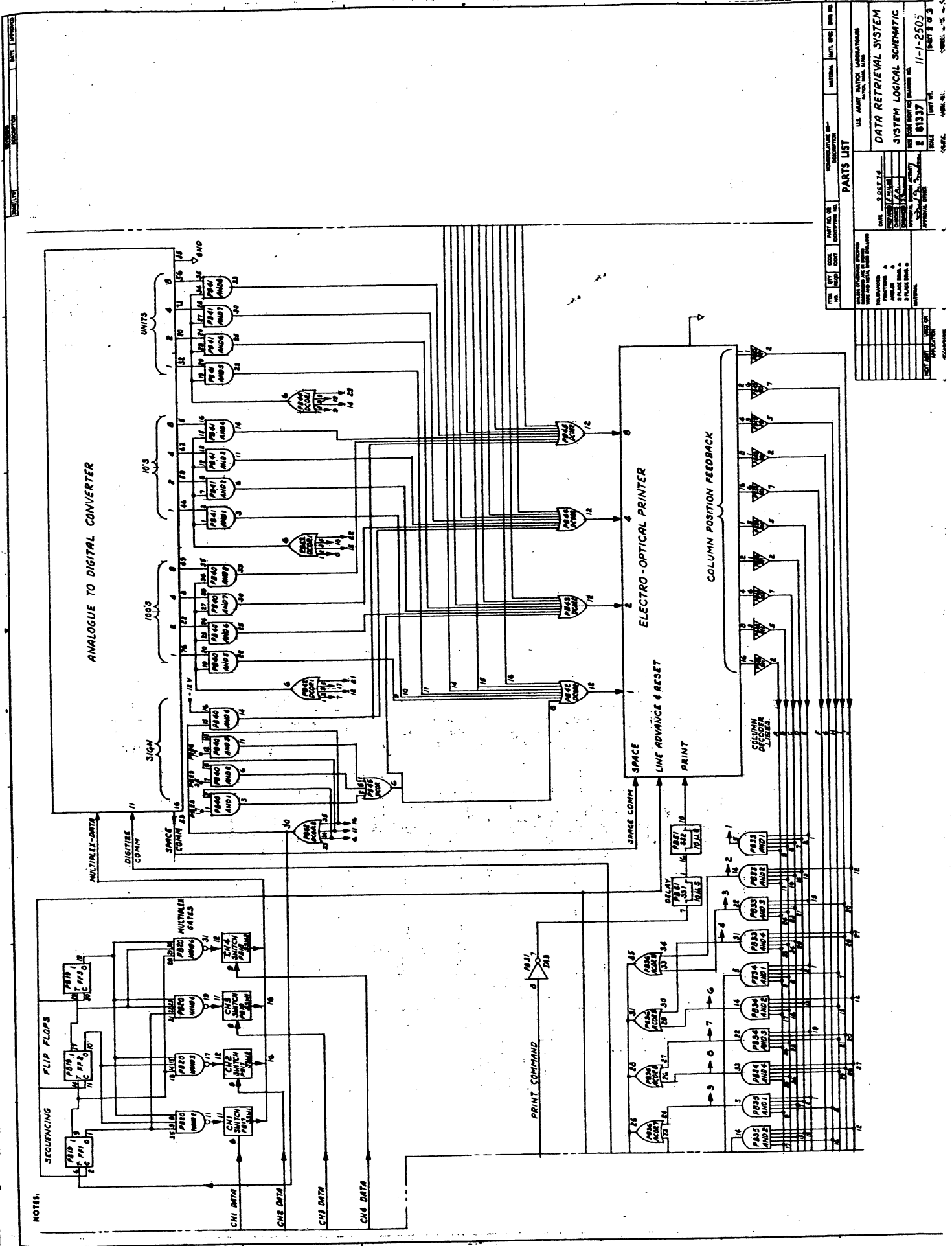
US ARMY NATICK LABORATORIES DRAWINGS

11-1-2505 THROUGH 11-1-2522

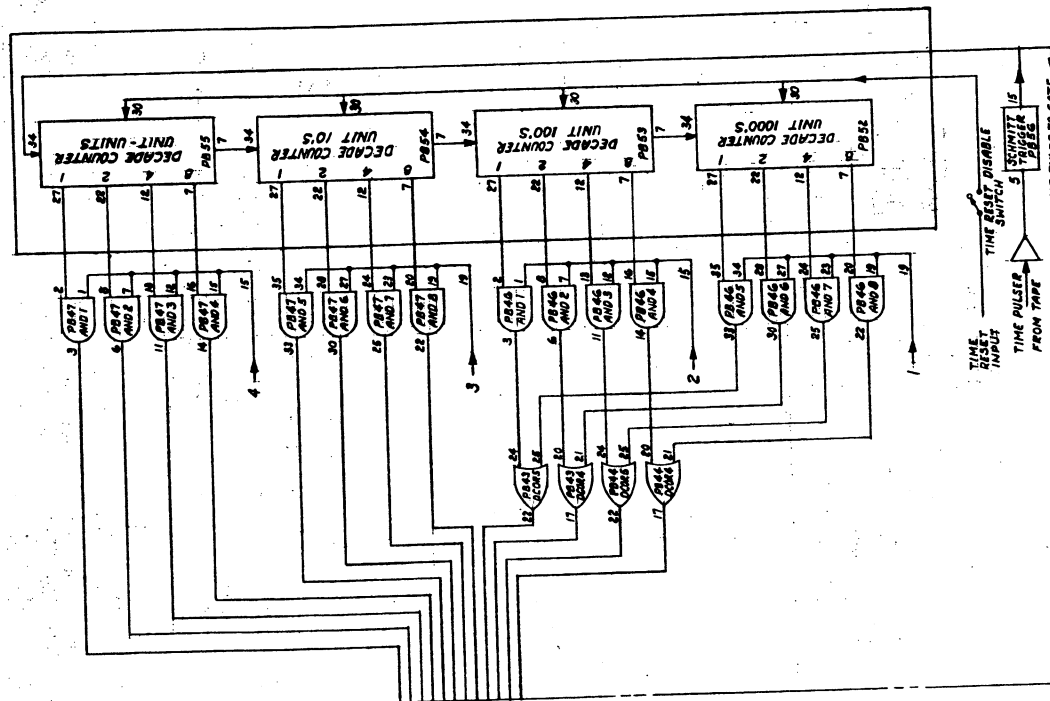


COLUMN GATE DECODER

[illegible]



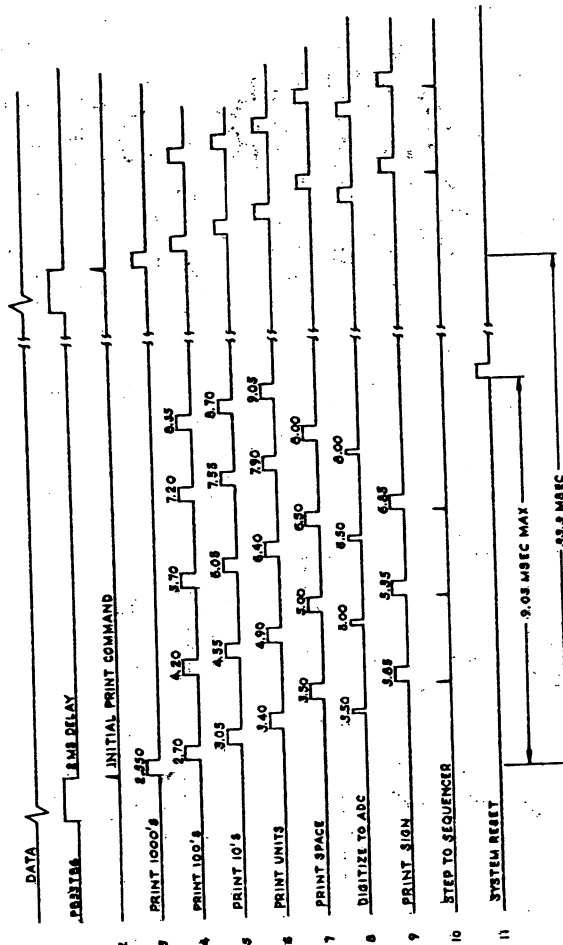
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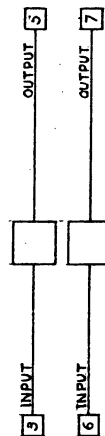
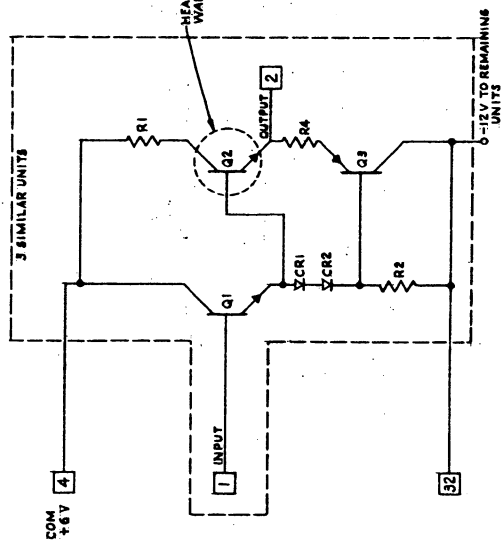


FUNCTION PRINT	TIME		μSEC		CH 1		μSEC		CH 2		μSEC		CH 3		μSEC		CH 4						
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COLUMN NO.																							

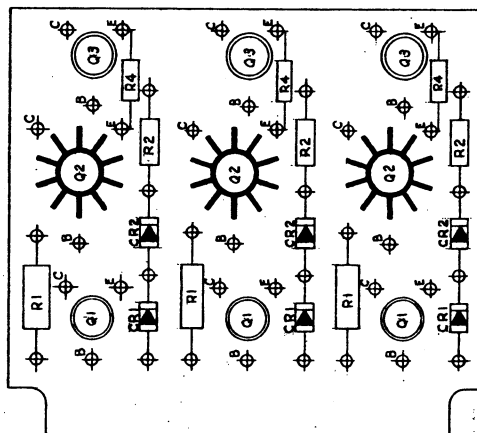
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<p>U.S. ARMY MATHEMATICS LABORATORY MATHEMATICS BRANCH WATERMAN, MASS. 0170</p>										
<p>DATA RETRIEVAL SYSTEM TIMING DIAGRAM</p>										
<p>SIZE: CODE IDENT NO. DRAWING NO. 11-1-2506 D 81337 SCALE: UNIT WT. SHEET 1 OF 1</p>										

NOTES:



SYM	COMPONENT	VALUE	TOL
CR1	HEAT SINK WAKEFIELD NF 204		
CR2	IN643A		
Q1	IN643A		
Q2	2N2219		
Q3	2N2219		
R1	RC22GF30J	33Ω	5%
R2	RC20GF81J	820Ω	5%
R4	RC20GF220J	22Ω	5%
PB1	RAYTHEON PLUG IN BOARD M881		



REV	DATE	APPROVED
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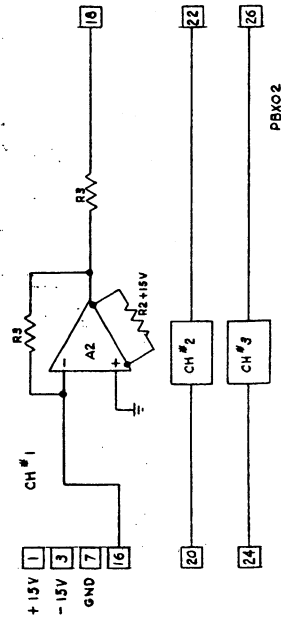
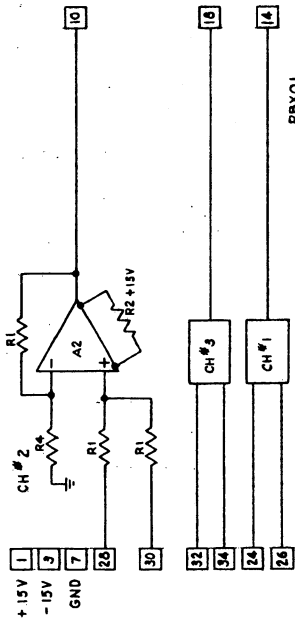
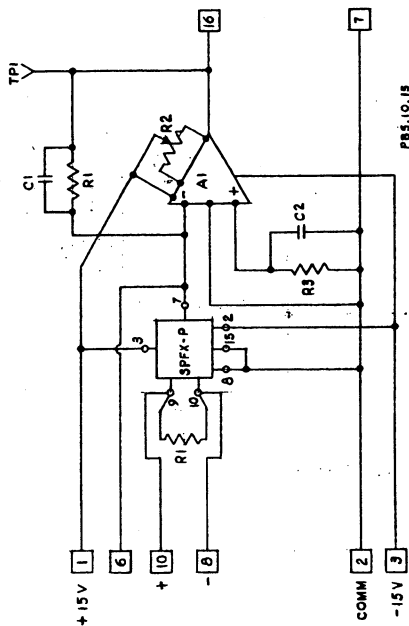
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NOTES:

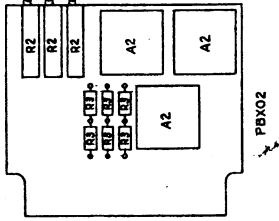
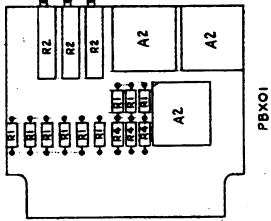
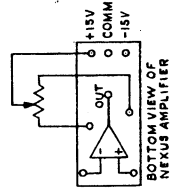
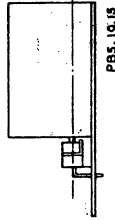
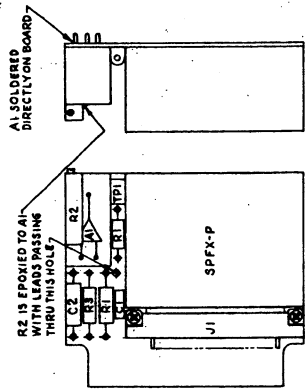
SYM	COMPONENT	VALUE	TOL
A1	NEXUS RESEARCH LABS DI-21		
C1	SPRAGUE 113D606C703031	60MFD	±1%
C2	SPRAGUE 113D606C703031	60MFD	±1%
C3	SPRAGUE 113D606C703031	60MFD	±1%
R1	MEPCO RN65C1001F	1.0K	1%
R2	MEPCO RN65C9011F	9.01K	1%
R3	BOURNS 200L-2-104K	100K	10%
R4	RN65B5113F	51.1K	1%
TPI	UNICITE 119437 TEST JACK		
PBI	RAYTHEON PLUG IN BOARD MBBI		

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NOTES:



SYM	COMPONENT	VALUE	TOL	QTY
A1	NEXUS RESEARCH LAB COA-12			1
A2	TELETYPE PHILBRICK 88-10A			4
SPFX-P	TRANSISTOR	18PF 10%		1
C1	ELMICO DM10-180J	0.1MF 10%		1
C2	SPRAGUE 118P103R22	20R 10%		1
R1	WPCO RN55C200SC	100K 10%		1
R2	BOURNS 200L-2-104	100K 10%		1
R3	WPCO RN55C200SC	100K 10%		1
R4	WPCO RN55C200SC	100K 10%		1
R5	WPCO RN55C200SC	100K 10%		1
R6	WPCO RN55C200SC	100K 10%		1
R7	WPCO RN55C200SC	100K 10%		1
R8	WPCO RN55C200SC	100K 10%		1
R9	WPCO RN55C200SC	100K 10%		1
R10	WPCO RN55C200SC	100K 10%		1
R11	WPCO RN55C200SC	100K 10%		1
R12	WPCO RN55C200SC	100K 10%		1
R13	WPCO RN55C200SC	100K 10%		1
R14	WPCO RN55C200SC	100K 10%		1
R15	WPCO RN55C200SC	100K 10%		1
R16	WPCO RN55C200SC	100K 10%		1
R17	WPCO RN55C200SC	100K 10%		1
R18	WPCO RN55C200SC	100K 10%		1
R19	WPCO RN55C200SC	100K 10%		1
R20	WPCO RN55C200SC	100K 10%		1
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R26	WPCO RN55C200SC	100K 10%		1
R27	WPCO RN55C200SC	100K 10%		1
R28	WPCO RN55C200SC	100K 10%		1
R29	WPCO RN55C200SC	100K 10%		1
R30	WPCO RN55C200SC	100K 10%		1
R31	WPCO RN55C200SC	100K 10%		1
R32	WPCO RN55C200SC	100K 10%		1
R33	WPCO RN55C200SC	100K 10%		1
R34	WPCO RN55C200SC	100K 10%		1
R35	WPCO RN55C200SC	100K 10%		1
R36	WPCO RN55C200SC	100K 10%		1
R37	WPCO RN55C200SC	100K 10%		1
R38	WPCO RN55C200SC	100K 10%		1
R39	WPCO RN55C200SC	100K 10%		1
R40	WPCO RN55C200SC	100K 10%		1
R41	WPCO RN55C200SC	100K 10%		1
R42	WPCO RN55C200SC	100K 10%		1
R43	WPCO RN55C200SC	100K 10%		1
R44	WPCO RN55C200SC	100K 10%		1
R45	WPCO RN55C200SC	100K 10%		1
R46	WPCO RN55C200SC	100K 10%		1
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R50	WPCO RN55C200SC	100K 10%		1
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R79	WPCO RN55C200SC	100K 10%		1
R80	WPCO RN55C200SC	100K 10%		1
R81	WPCO RN55C200SC	100K 10%		1
R82	WPCO RN55C200SC	100K 10%		1
R83	WPCO RN55C200SC	100K 10%		1
R84	WPCO RN55C200SC	100K 10%		1
R85	WPCO RN55C200SC	100K 10%		1
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R93	WPCO RN55C200SC	100K 10%		1
R94	WPCO RN55C200SC	100K 10%		1
R95	WPCO RN55C200SC	100K 10%		1
R96	WPCO RN55C200SC	100K 10%		1
R97	WPCO RN55C200SC	100K 10%		1
R98	WPCO RN55C200SC	100K 10%		1
R99	WPCO RN55C200SC	100K 10%		1
R100	WPCO RN55C200SC	100K 10%		1

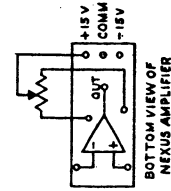
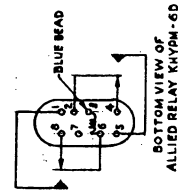
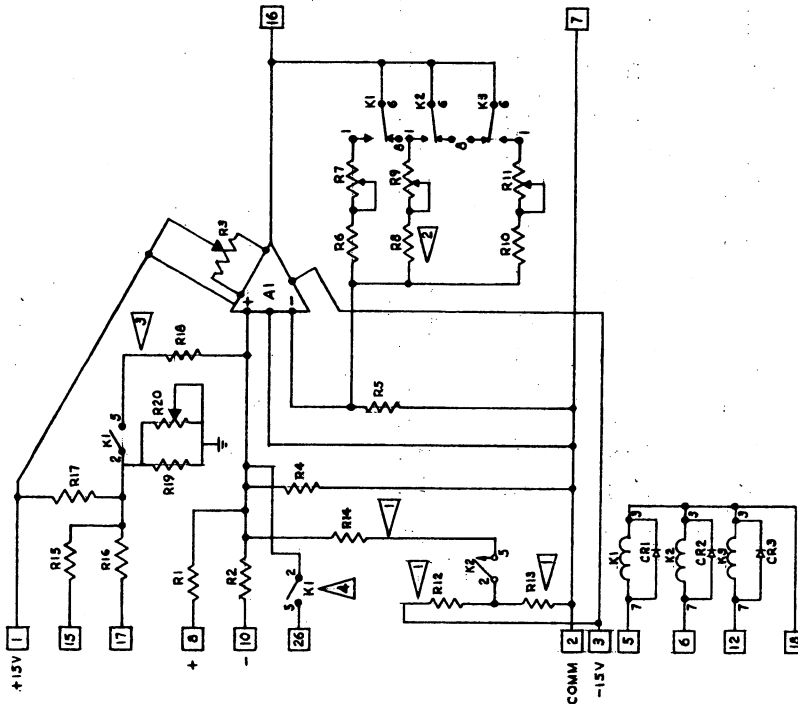


ITEM NO.	QTY	CODE	DESCRIPTION	PART NO. OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	UNIT	QTY	DATE	APPROVED
1	1	81337	DATA RETRIEVAL SYSTEM							
2	1	81337	ARBITRARY FUNCTION							
3	1	81337	PB5, PB10, PB15, PBX01, PBX02							
4	1	81337	SIZE CODE IDENT NO. DRAWING NO.							
5	1	81337	APPROVAL DESIGN ACTIVITY							
6	1	81337	APPROVAL OTHER							

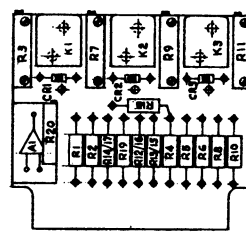
U.S. ARMY MATER LABORATORIES	DATE	9 OCT 74
DATA RETRIEVAL SYSTEM	PREPARED BY	81337
ARBITRARY FUNCTION	CHECKED BY	81337
PB5, PB10, PB15, PBX01, PBX02	ENGINEER	81337
SIZE CODE IDENT NO. DRAWING NO.	APPROVAL DESIGN ACTIVITY	81337
D 81337	APPROVAL OTHER	81337
SCALE	UNIT	WT.
SHEET	OF	11-1-2511

REVISION	DATE	APPROVED
1		

NOTES:



- 1 - R15, R16 AND R17 ARE USED ON THE PLUG IN BOARD IN THE TEMPERATURE CHANNEL (P84)
- 2 - R8 IS RNE5C200F 20K 1% ON THE PLUG IN BOARD IN THE STATIC LOAD CHANNEL (P89)
- 3 - ON P89 ONLY
- 4 - ON P84 AND P814 ONLY



SYM	COMPONENT	VALUE	TOL
K1	ALLIED CONTROL KHYPM-60-12D		
K2	ALLIED CONTROL KHYPM-60-12D		
K3	ALLIED CONTROL KHYPM-60-12D		
R1	MEPCO RNE5C200ZC	20K	25%
R2	MEPCO RNE5C200ZC	20K	25%
R3	BOURNS 200L-E-104	100K	10%
R4	MEPCO RNE5C1000C	1K	25%
R5	MEPCO RNE5C1000C	2K	25%
R6	MEPCO RNE5C1692F	2.49K	1%
R7	BOURNS 200L-E-103	10K	10%
R8	MEPCO RNE5C1111F	8.1K	1%
R9	BOURNS 200L-E-302	3K	1%
R10	MEPCO RNE5C3832F	38.3K	10%
R11	BOURNS 200L-E-103	10K	10%
R12	MEPCO RNE5C4816C	2.48K	25%
R13	MEPCO RNE5C4816C	4.89K	25%
R14	MEPCO RNE5C1962C	19.6K	25%
R15	MEPCO RNE5C1962C	19.6K	25%
R16	MEPCO RNE5C1962C	2K	25%
R17	MEPCO RNE5C1962C	19.6K	25%
R18	MEPCO RNE5C1962C	19.6K	25%
R19	SPRAGUE RN45C	590Ω	25%
R20	BOURNS 200L-E-302	3K	1%
CR1	IN4838		
CR2	IN4838		
CR3	IN4838		
A1	NEXUS RESEARCH LABS CDA-1/2 &		
P81	RAYTHEON PLUG IN BOARD P8B1		

PARTS LIST

ITEM NO.	QTY	CODE	IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	MAT. SPEC.	DWG NO.
1	1			ALLIED CONTROL KHYPM-60-12D			
2	1			ALLIED CONTROL KHYPM-60-12D			
3	1			ALLIED CONTROL KHYPM-60-12D			
4	1			MEPCO RNE5C200ZC			
5	1			MEPCO RNE5C200ZC			
6	1			BOURNS 200L-E-104			
7	1			MEPCO RNE5C1000C			
8	1			MEPCO RNE5C1000C			
9	1			MEPCO RNE5C1692F			
10	1			BOURNS 200L-E-103			
11	1			MEPCO RNE5C1111F			
12	1			BOURNS 200L-E-302			
13	1			MEPCO RNE5C3832F			
14	1			BOURNS 200L-E-103			
15	1			MEPCO RNE5C4816C			
16	1			MEPCO RNE5C4816C			
17	1			MEPCO RNE5C1962C			
18	1			MEPCO RNE5C1962C			
19	1			MEPCO RNE5C1962C			
20	1			MEPCO RNE5C1962C			
21	1			SPRAGUE RN45C			
22	1			BOURNS 200L-E-302			
23	1			IN4838			
24	1			IN4838			
25	1			IN4838			
26	1			NEXUS RESEARCH LABS CDA-1/2 &			
27	1			RAYTHEON PLUG IN BOARD P8B1			

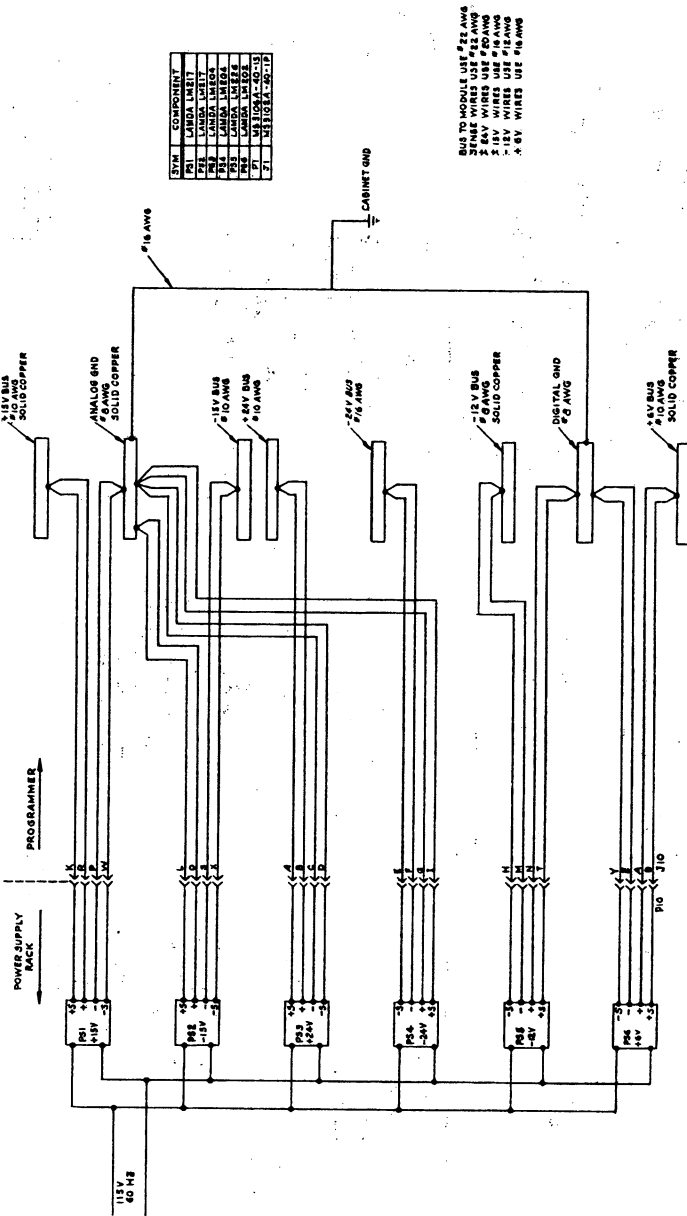
U.S. ARMY MATCO LABORATORIES
MATCO, MALE, 01940

DATA RETRIEVAL SYSTEM
OUTPUT AMPLIFIER
P84, P89, P814

DATE 9 OCT 74
PREPARED BY
CHECKED BY
APPROVED BY
APPROVAL OTHER
SCALE
UNIT WT
SHEET OF

NOTES:

DATE	DESCRIPTION	DATE	APPROVED
1/1/74			

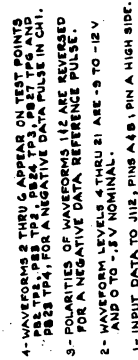


ITEM	DESCRIPTION
P1	15V BUS SOLID COPPER
P2	12V BUS SOLID COPPER
P3	8V BUS SOLID COPPER
P4	24V BUS SOLID COPPER
P5	5V BUS SOLID COPPER
P6	5V BUS SOLID COPPER

BUS TO MODULE USE #16 AWG
SENSE WIRES USE #22 AWG
24V WIRES USE #10 AWG
12V WIRES USE #12 AWG
8V WIRES USE #14 AWG
5V WIRES USE #16 AWG

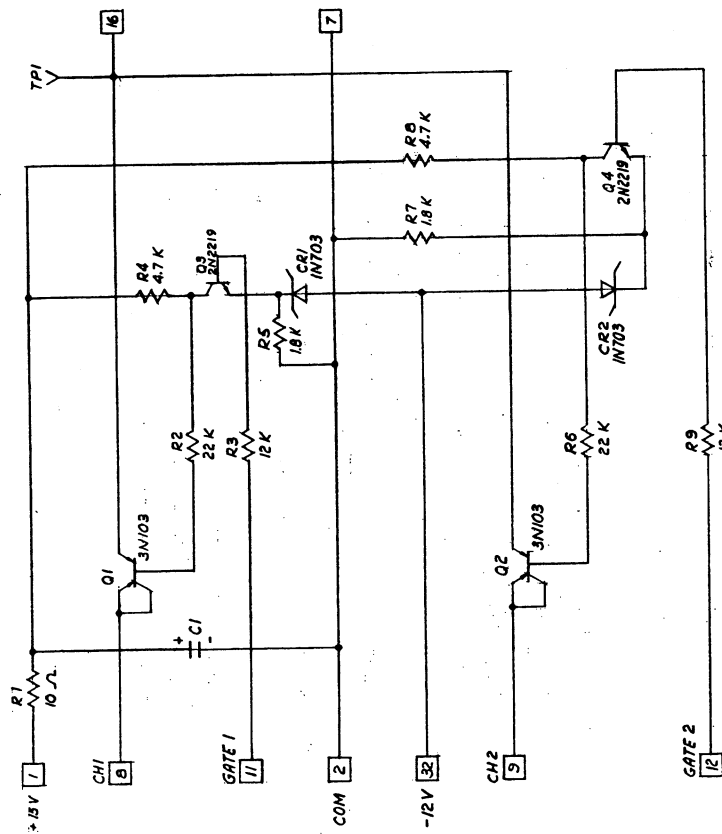
ITEM NO.	QTY	CODE	DATE	NO. OF	DESCRIPTION	MATERIAL	DATE	NO.
PARTS LIST								
U.S. ARMY MEDICAL LABORATORIES								
DATA RETRIEVAL SYSTEM								
POWER SUPPLY CONNECTIONS								
DATE 9 OCT 74								
DRAWN BY [Signature]								
CHECKED BY [Signature]								
APPROVED BY [Signature]								
11-1-2513								

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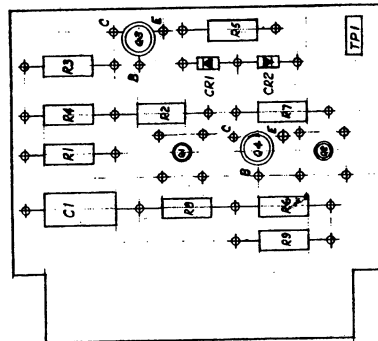


PARTS LIST										U.S. ARMY WATER LABORATORIES WATER WORKS, WASH DC										DATA RETRIEVAL SYSTEM TROUBLE SHOOTING TIMING DIAGRAM										SEE PAGE 10 OF 10 E 81337 11-1-2516										11-1-2516																																																																																																																																																															
1. NO.		2. DTG		3. CODE		4. SORT		5. DATE		6. IN		7. TO		8. DISPATCHING TO		9. DISPOSITION		10. OR		11. MATERIAL		12. DATE		13. TIME		14. DATE		15. TIME		16. DATE		17. TIME		18. DATE		19. TIME		20. DATE		21. TIME		22. DATE		23. TIME		24. DATE		25. TIME		26. DATE		27. TIME		28. DATE		29. TIME		30. DATE		31. TIME		32. DATE		33. TIME		34. DATE		35. TIME		36. DATE		37. TIME		38. DATE		39. TIME		40. DATE		41. TIME		42. DATE		43. TIME		44. DATE		45. TIME		46. DATE		47. TIME		48. DATE		49. TIME		50. DATE		51. TIME		52. DATE		53. TIME		54. DATE		55. TIME		56. DATE		57. TIME		58. DATE		59. TIME		60. DATE		61. TIME		62. DATE		63. TIME		64. DATE		65. TIME		66. DATE		67. TIME		68. DATE		69. TIME		70. DATE		71. TIME		72. DATE		73. TIME		74. DATE		75. TIME		76. DATE		77. TIME		78. DATE		79. TIME		80. DATE		81. TIME		82. DATE		83. TIME		84. DATE		85. TIME		86. DATE		87. TIME		88. DATE		89. TIME		90. DATE		91. TIME		92. DATE		93. TIME		94. DATE		95. TIME		96. DATE		97. TIME		98. DATE		99. TIME		00. DATE	
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NOTES:



SYM	COMPONENT	VALUE	TOL
CR1	DIODE 1N703		
CR2	DIODE 1N703		
C1	SPARE	50007X00012	100NF
R1	RC20GF100J	10.0K	5%
R2	RC20GF23J	22K	5%
R3	RC20GF12J	12K	5%
R4	RC20GF47J	4.7K	5%
R5	RC20GF18J	1.8K	5%
R6	RC20GF23J	22K	5%
R7	RC20GF18J	1.8K	5%
R8	RC20GF47J	4.7K	5%
R9	RC20GF12J	12K	5%
Q1	3N103		
Q2	3N103		
Q3	2N2219		
Q4	2N2219		

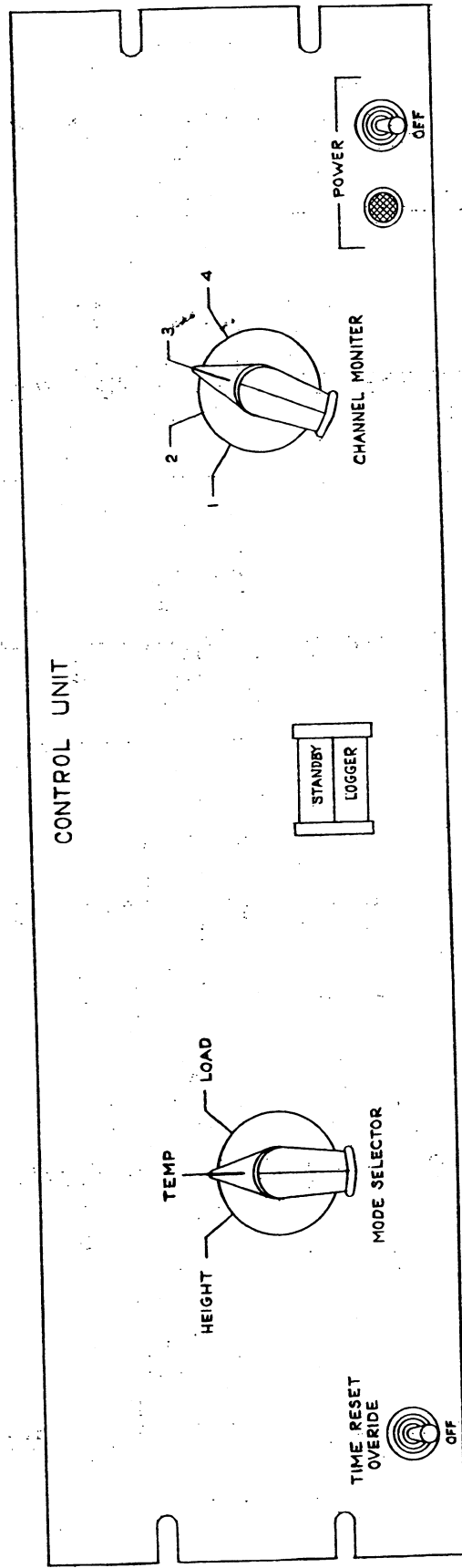
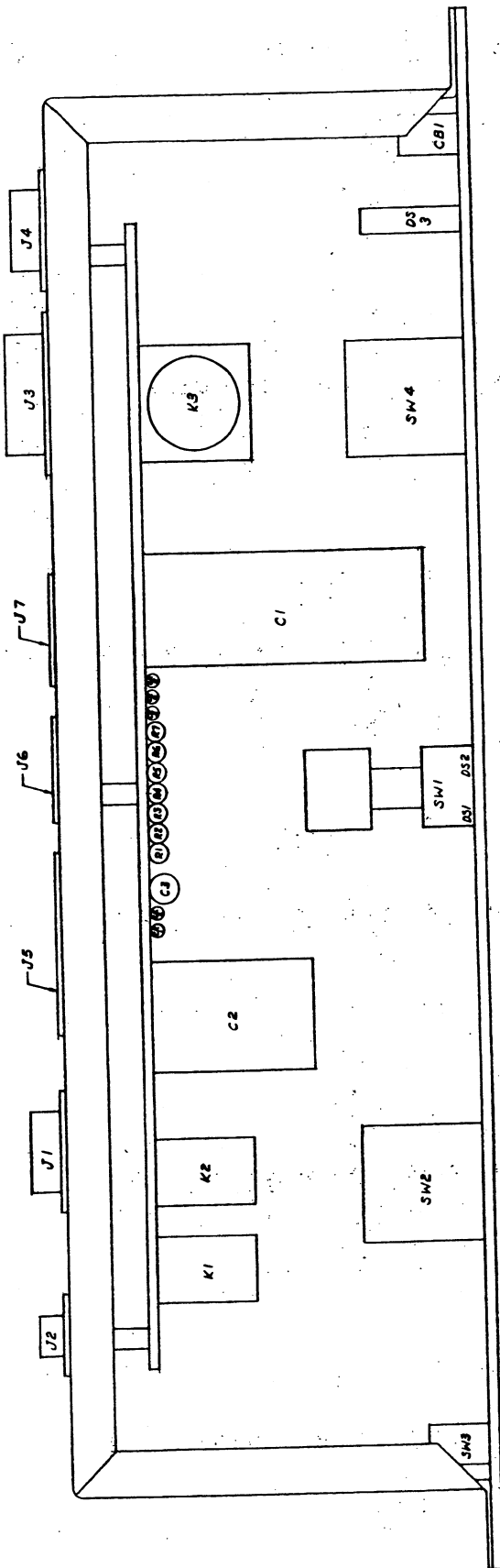


PARTS LIST

ITEM	QTY	CODE	DESCRIPTION	UNIT	QTY	UNIT	QTY	UNIT	QTY	UNIT
1	1	CR1	DIODE 1N703	DIODE	1	DIODE	1	DIODE	1	DIODE
2	1	CR2	DIODE 1N703	DIODE	1	DIODE	1	DIODE	1	DIODE
3	1	C1	SPARE	CAPACITOR	1	CAPACITOR	1	CAPACITOR	1	CAPACITOR
4	1	R1	RC20GF100J	RESISTOR	1	RESISTOR	1	RESISTOR	1	RESISTOR
5	1	R2	RC20GF23J	RESISTOR	1	RESISTOR	1	RESISTOR	1	RESISTOR
6	1	R3	RC20GF12J	RESISTOR	1	RESISTOR	1	RESISTOR	1	RESISTOR
7	1	R4	RC20GF47J	RESISTOR	1	RESISTOR	1	RESISTOR	1	RESISTOR
8	1	R5	RC20GF18J	RESISTOR	1	RESISTOR	1	RESISTOR	1	RESISTOR
9	1	R6	RC20GF23J	RESISTOR	1	RESISTOR	1	RESISTOR	1	RESISTOR
10	1	R7	RC20GF18J	RESISTOR	1	RESISTOR	1	RESISTOR	1	RESISTOR
11	1	R8	RC20GF47J	RESISTOR	1	RESISTOR	1	RESISTOR	1	RESISTOR
12	1	R9	RC20GF12J	RESISTOR	1	RESISTOR	1	RESISTOR	1	RESISTOR
13	1	Q1	3N103	TRANSISTOR	1	TRANSISTOR	1	TRANSISTOR	1	TRANSISTOR
14	1	Q2	3N103	TRANSISTOR	1	TRANSISTOR	1	TRANSISTOR	1	TRANSISTOR
15	1	Q3	2N2219	TRANSISTOR	1	TRANSISTOR	1	TRANSISTOR	1	TRANSISTOR
16	1	Q4	2N2219	TRANSISTOR	1	TRANSISTOR	1	TRANSISTOR	1	TRANSISTOR

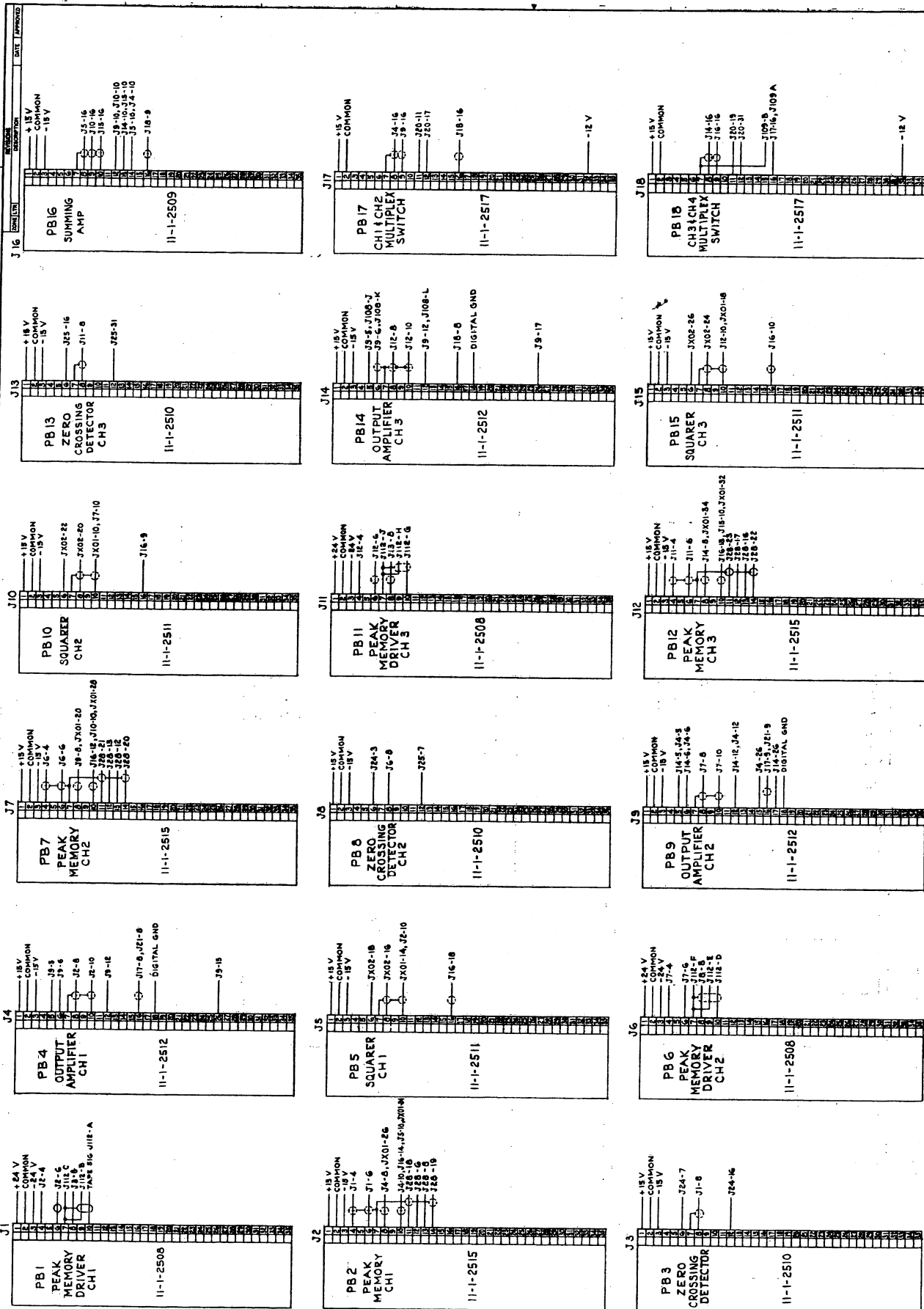
U.S. ARMY RESEARCH LABORATORIES
 DATA RETRIEVAL SYSTEM
 PART 18
 11-1-2517

NOTES:



ITEM NO.	QTY	CODE	DESCRIPTION	DATE NO. OF	REVISIONS	DATE	BY	REVISIONS	DATE	BY
1	1		DATA RETRIEVAL SYSTEM							
2	1		CONTROL PANEL							
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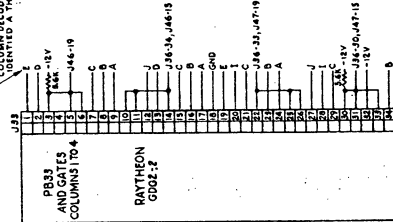
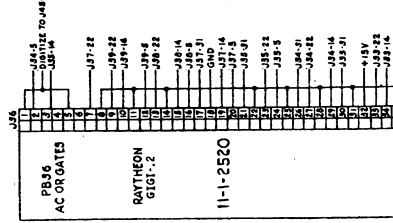
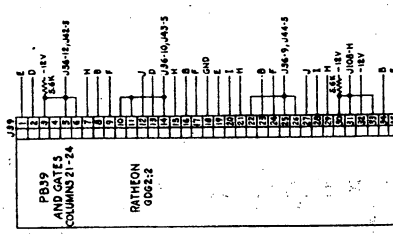
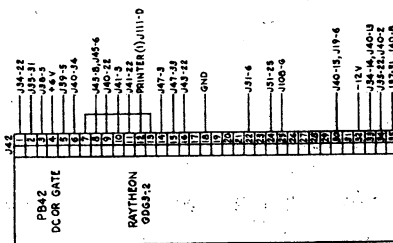
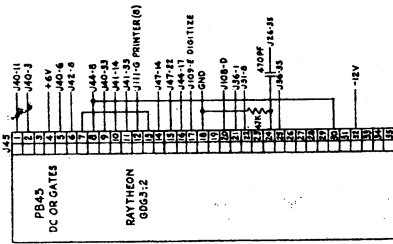
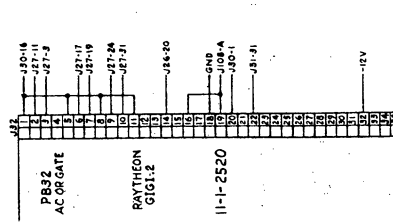
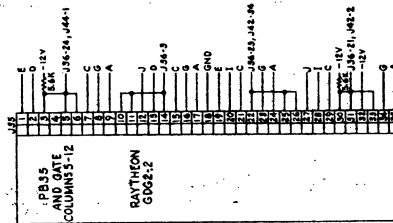
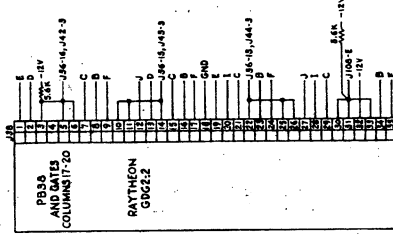
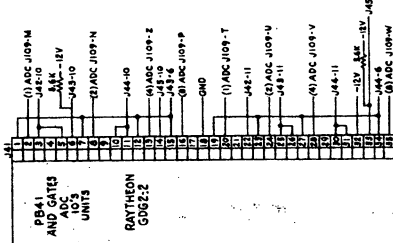
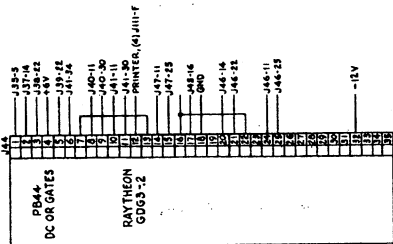
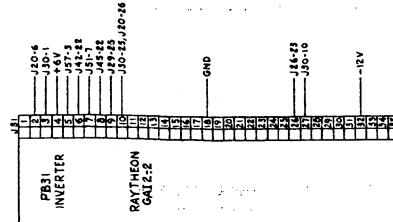
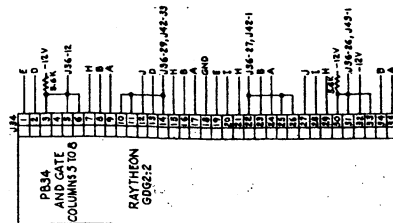
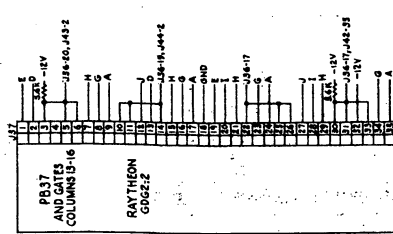
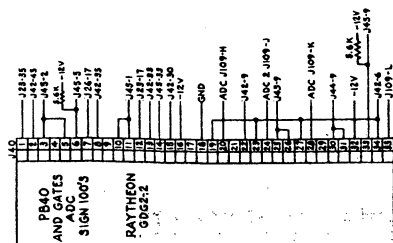
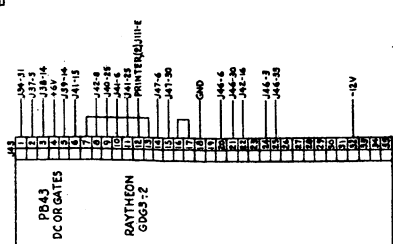
NOTES:



ITEM	QTY	CODE	DESCRIPTION	PART NO. OR IDENT.	MANUFACTURING OR IDENT.	MATERIAL	DATE	APPROVED
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ITEM	QTY	CODE	DESCRIPTION	PART NO. OR IDENT.	MANUFACTURING OR IDENT.	MATERIAL	DATE	APPROVED
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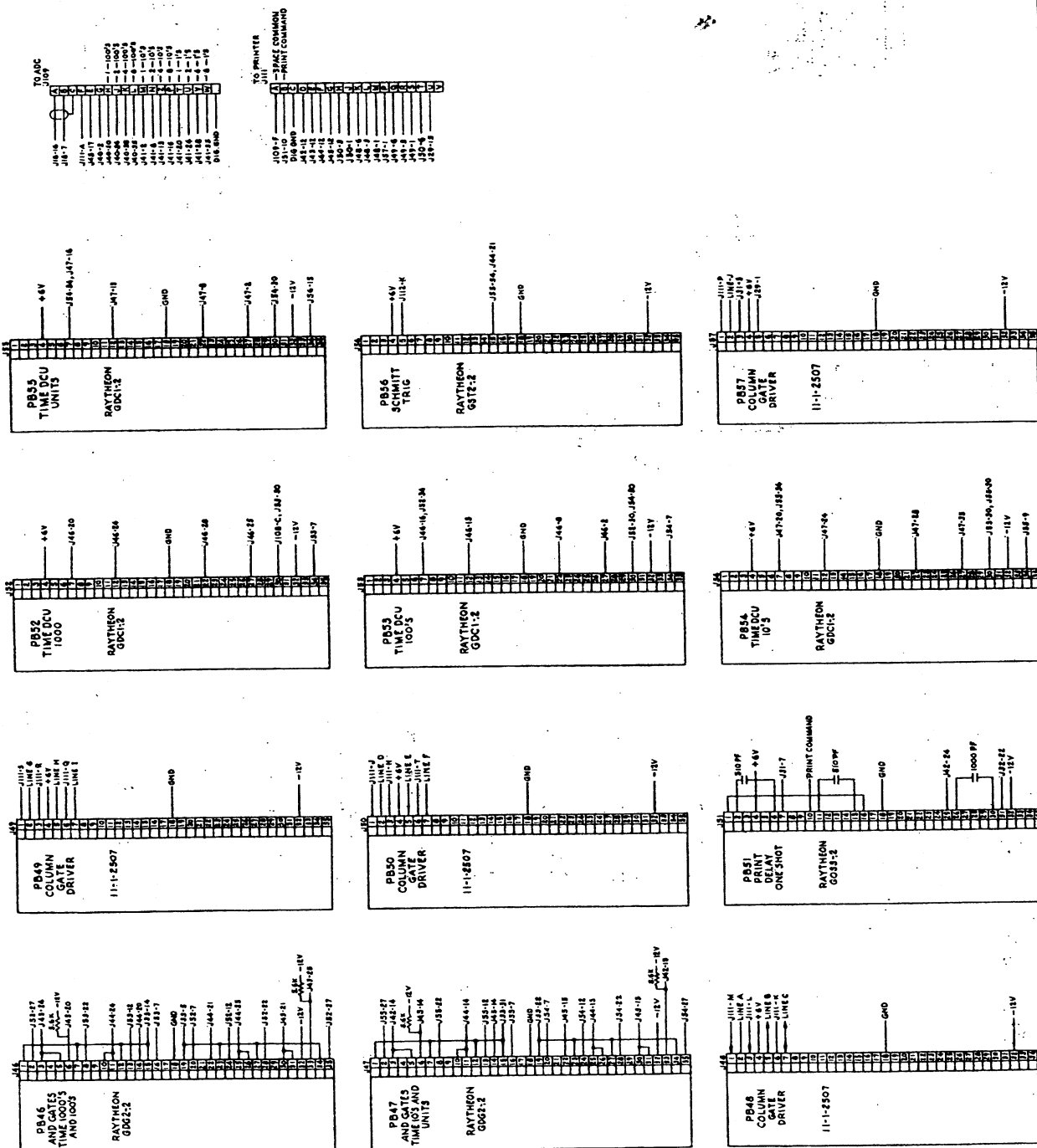
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15	1	1	1	1	1	1	1	1
16	1	1	1	1	1	1	1	1



—LETTERS CORRESPOND TO
COLUMN DECODER LINES
IDENTIFIED ABOVE.

[illegible]

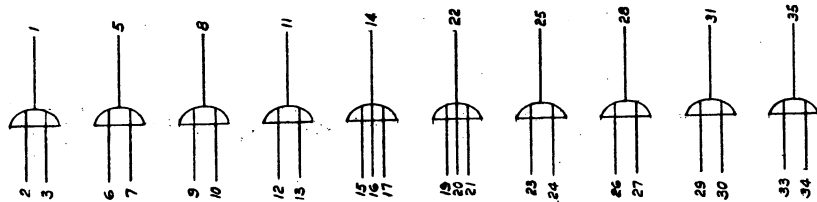
NOTES:



NOTES:

[illegible]

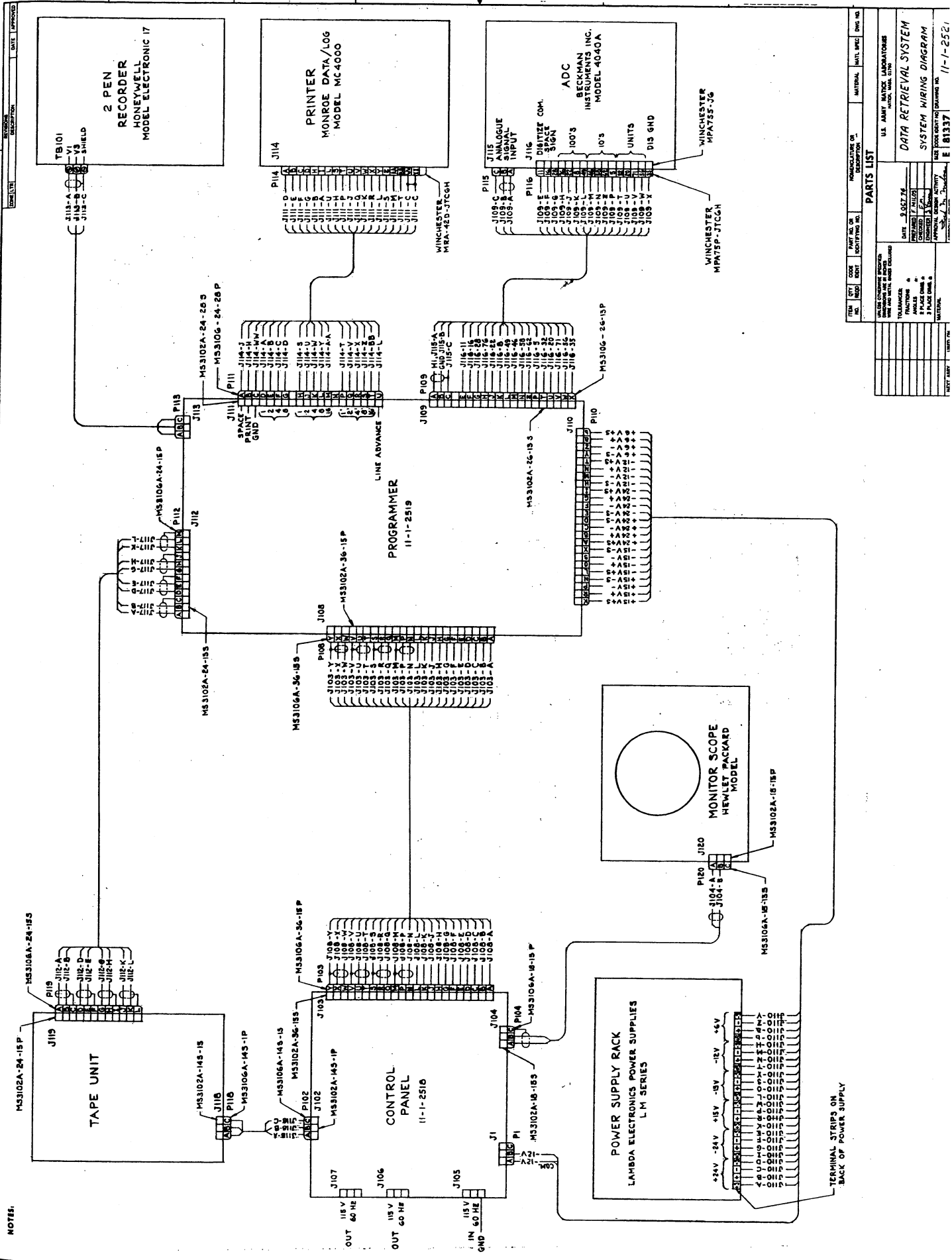
NOTES:
1. THIS BOARD IS A RAYTHEON GIGI-2 WITH THE DIODES REVERSED AND RA & RB REPLACED WITH 47K RESISTORS.



SYM	COMPONENT	VALUE	TOL
CA	CAPACITOR	390Pf	±10%
CB	CAPACITOR	390Pf	±10%
CRA	RAYTHEON PBC503050		
CRB	RAYTHEON PBC503050		
CRC	RAYTHEON PBC503050		
CRD	RAYTHEON PBC503050		
RA	RC206F473J	47 K	5%
RB	RC206F473J	47 K	5%

DATE	DESCRIPTION	DATE	APPROVED

ITEM NO.	QTY	CODE	IDENT	PART NO. OR IDENTIFYING NO.	DESCRIPTION	MATERIAL	MATL SPEC	DWG NO.
PARTS LIST								
U.S. ARMY MATCOX LABORATORIES MATCOX BANG. 01760								
DATE 9 OCT 74 PREPARED P. M. 11/25 CHECKED P. M. 11/25 ENGINEER P. M. 11/25								
DATA RETRIEVAL SYSTEM AC OR GATE NEGATIVE INPUT PB36								
SIZE CODE IDENT NO. DRAWING NO. D 81337 11-1-2520								
APPROVAL OTHERS SCALE UNIT WT. SHEET OF								



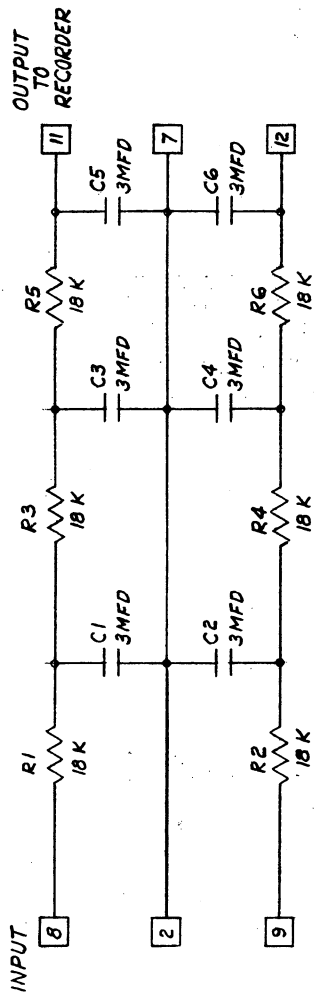
NOTES:

PARTS LIST		MANUFACTURER OF		MATERIAL		DATE	
ITEM NO.	QTY	CODE	DESCRIPTION	IDENTIFY NO.	DATE	DATE	DATE
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3	1		WIRE				
4	1		WIRE				
5	1		WIRE				
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U.S. ARMY MATERIEL LABORATORIES ATTENTION: DATA RETRIEVAL SYSTEM		PARTS LIST	
DATE 3-22-74		DATE	
PREPARED BY MILLER		PREPARED BY	
CHECKED BY		CHECKED BY	
DRAWN BY		DRAWN BY	
INSTRUMENTED BY		INSTRUMENTED BY	
APPROVAL		APPROVAL	
DESIGN		DESIGN	
ACTIVITY		ACTIVITY	
E 81337		E 81337	
11-1-2521		11-1-2521	

NOTES:

SYM	COMPONENT	VALUE	TOL
C1	SPRAGUE 118P30592S2	3 MFD	10 %
C2	SPRAGUE 118P30592S2	3 MFD	10 %
C3	SPRAGUE 118P30592S2	3 MFD	10 %
C4	SPRAGUE 118P30592S2	3 MFD	10 %
C5	SPRAGUE 118P30592S2	3 MFD	10 %
C6	SPRAGUE 118P30592S2	3 MFD	10 %
R1	RC20GF183J	18 K	5 %
R2	RC20GF183J	18 K	5 %
R3	RC20GF183J	18 K	5 %
R4	RC20GF183J	18 K	5 %
R5	RC20GF183J	18 K	5 %
R6	RC20GF183J	18 K	5 %



ITEM NO.

QTY REQD

CODE IDENT

PART NO. OR IDENTIFYING NO.

NOMENCLATURE OR DESCRIPTION

MATERIAL

NATL SPEC

DWG NO.

DATE

PREPARED

CHECKED

APPROVED

APPROVAL OTHER

U.S. ARMY NATCH LABORATORIES

NATCH DMR 0190

DATA RETRIEVAL SYSTEM

RECORDER FILTER

PB21

SIZE CODE ENST NO DRAWING NO.

D 81337

11-1-2522